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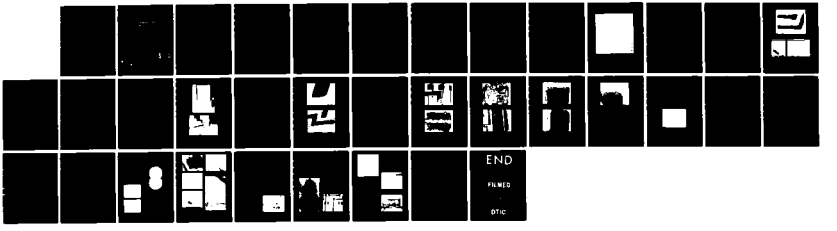

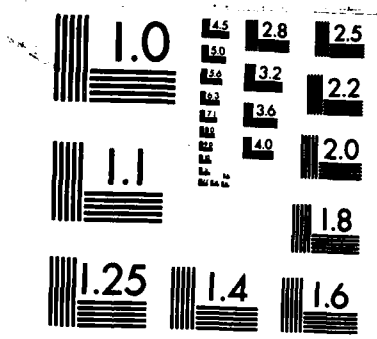

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HIGH TEMPERATURE ELECTRONICS TECHNOLOGY

LIFE TEST REPORT
FINAL REPORT - CDRL Item A003

MARCH 1985

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19. ABSTRACT (Continue on reverse if necessary and identify by block number)

This report presents the results of a series of life tests of silicon Integrated Injection Logic (I^2L) microcircuits designed to operate for long periods at temperatures as high as 300° C. The technology needed to design and fabricate these microcircuits was previously developed under Contract N00173-79-C-0010. Two life tests were conducted: an operating-life test at 300° C and a nonoperating-life test at 360° C. Ten chip packages, each containing four identical ring oscillator/counter test circuits, were tested at each temperature. A total of 80 microcircuits were fabricated using two different metallization processes. None of the 300° C test specimens failed; 24 circuits of the 40 completed 3206 hours, and 16 completed 2342 hours. Of the 40 circuits tested at 360° C, 4 experienced "infant mortality" failure at about 1000 hours, but the remaining 36 circuits ran without failure for 2618 hours. Posttest analysis indicates that metallization deterioration began with scattered formation of voids and extruded gold crystals in the connecting runs. The overall test results were considered very encouraging, and operational life is estimated to be more than 18,000 hours at 300° C. Continued development efforts are recommended.

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11. Life Test Report

FOREWORD

This report covers the life testing of silicon Integrated Injection Logic (I^2L) microcircuits developed for potential on-engine electronic controls for advanced aircraft gas turbines. The program was conducted by the Aircraft Engine Business Group of the General Electric Company for the Naval Research Laboratory under Naval Air Systems Command sponsorship.

The life test effort reported herein was performed during the period October 1983 through June 1984. The Navy Scientific Officer was Dr. A. Christou, NRL Code 6815. The General Electric Program Manager was Mr. Mason D. Marvin; the semiconductor development work at the Electronics Laboratory in Syracuse, New York was performed under the direction of Dr. Donald J. LaCombe. Mr. James E. Hurtle provided overall program technical direction consistent with the needs of advanced digital controls.

The development of the life test microcircuits and particularly the metallization development was accomplished as part of a prior program conducted under Contract N00173-79-C-0010, also under the technical direction of the Naval Research Laboratory. The results of that program are reported separately.

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

1.0 INTRODUCTION

This report presents the results of a series of life tests of microcircuits designed to operate for long periods of time at temperatures as high as 300° C. The technology needed to design and fabricate these microcircuits was developed on an earlier Navy sponsored program (Contract N00173-79-C-0010). This life test program is a continuation of that effort with the objective of demonstrating that the new, high-temperature microcircuit technology is adequate for the intended purpose: aircraft engine-mounted electronics.

A brief technical summary of the associated prior development efforts is presented in the Appendix of this report and provides useful background to the design and fabrication of the microcircuits tested and evaluated in this program. During Phase I of the prior program, exploratory tests indicated that microcircuits using Integrated Injection Logic (I^2L) are capable of functioning at 300° C (Reference 1). Life tests of I^2L circuits demonstrated that the basic technology was capable of providing long-life microcircuits at that temperature but that life was limited by the metallization system. The aluminum systems commonly used for metallization are limited by electromigration and ohmic contact degradation at high temperatures. Extensive development work on the previous contract resulted in three candidate metallization systems which showed promise of long life at 300° C. Test wafers consisting of medium-scale integration (MSI) complexity, ring-oscillator/binary-counter circuits were processed up to the metallization step and were available for use on this life test.

During this life testing, fabrication of the wafers was to be completed using each of the three candidate metal systems, followed by chip packaging and life testing at two different conditions. One condition involved an operating-life test at 300° C, and the other was a nonoperating-life test at 360° C. Both tests were to continue until at least half of the circuits failed or for 2000 hours, whichever occurred first. As a result of the tests, conclusions were to be drawn concerning the minimum lifetimes to be expected for microcircuits fabricated using the technologies.

Section 2.0 of this report describes the test circuits, including design, fabrication, and packaging. Section 3.0 describes the life tests, including the test facility and the test procedures. Section 4.0 presents the results of the life tests. Section 5.0 presents the results of a physical analysis of several samples which survived the tests. Finally, Section 6.0 contains a discussion of the results and presents the conclusions.

2.0 DESCRIPTION OF TEST SAMPLES

2.1 LIFE-TEST CIRCUIT

The life-test circuit was contained in sector 4 of the E115 test mask which included the following elements:

- Four independent, I^2L, MSI complexity, life-test circuits...Each circuit consists of a seven-stage ring oscillator and four-bit binary counter. Clock signals generated by the ring oscillator are divided by a factor of 16 using four toggle flipflops. The resulting signal is buffered and brought out to a pad for monitoring.

- A bottom metal continuity-test circuit...This element involves a serpentine metal run 9 um wide with 9-um spacing. The total length is 34 mm on top of oxide steps consisting of alternating base on P-ISO and emitter on N sinker diffusions.

- A metal-to-metal contact continuity chain...The objective of this element is to evaluate a large number of vias between top and bottom metal levels. Each via is 8 x 8 um with 2-um top metal overlap and a 4-um bottom metal overlap. The serpentine is tapped out after 60, 120, 240, and 660 vias.

- An I^2L evaluation gate...In this element all necessary connections to a pair of dual-collector I^2L gates are brought out to the pads for process evaluation.

Only the first of these elements was used for the life-test program. However, the I^2L evaluation gate was used for diagnostic purposes in trouble-shooting circuits which did not function. The E115 test mask contained six sectors total, each addressing different aspects of the metallization development. Figure 1 is a microphotograph of sector 4 with the component identified. This sector was used to fabricate the microcircuits used for the life test.

2.2 METALLIZATION VARIATIONS

E115 wafers were metallized with three different metal systems. All three metal systems had the structure shown in Figure 2; the differences between systems were in the manner in which the gold layer was deposited.

- Wafers with "normal gold" were sputtered with gold with no attempt to control the wafer temperature during sputtering.

- Wafers with "high-temperature gold" were first sputtered with a 50-nm layer of normal gold, followed by 450 nm of gold sputtered while the wafer was held at 350° C.

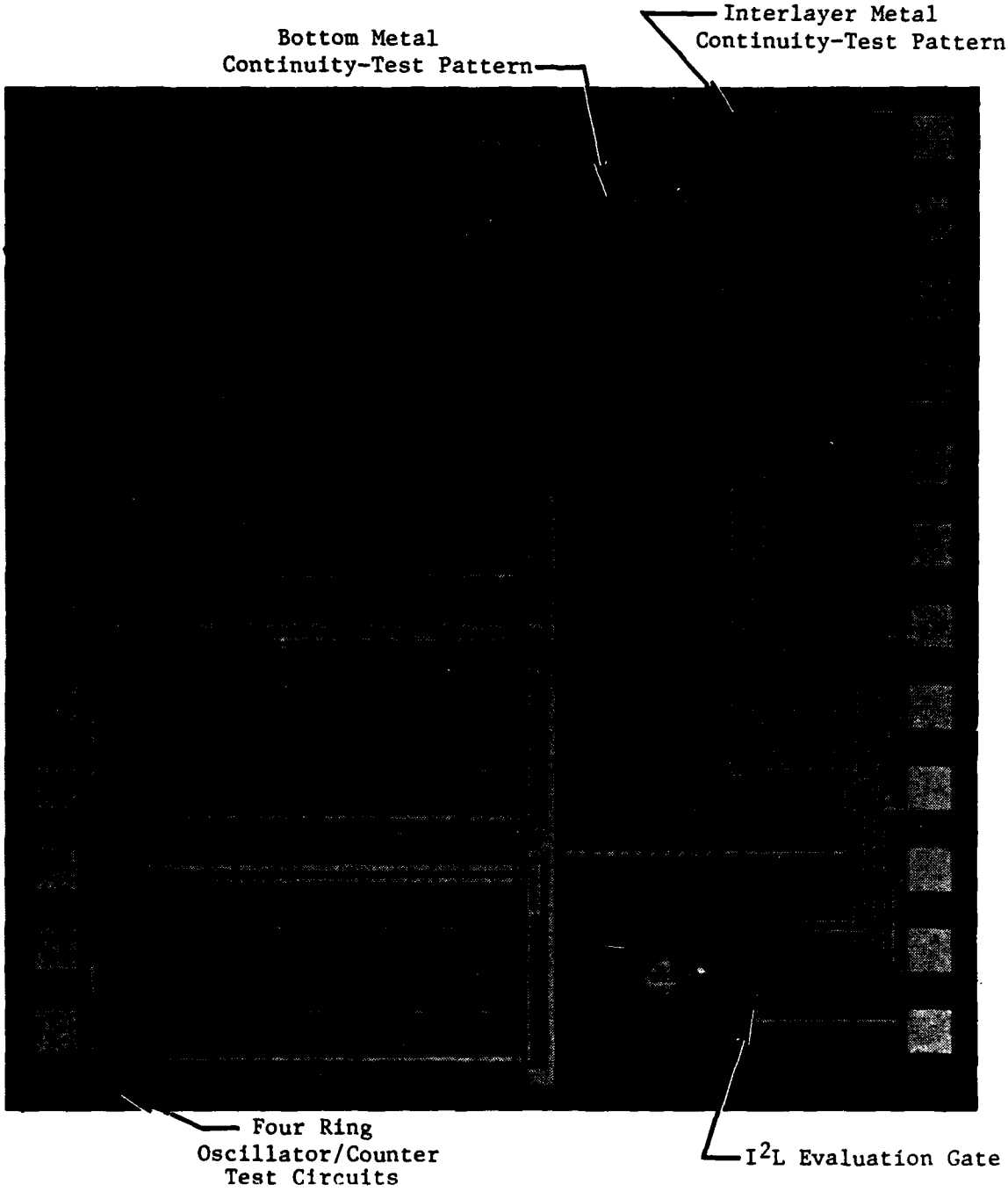


Figure 1. Life-Test Microcircuits.

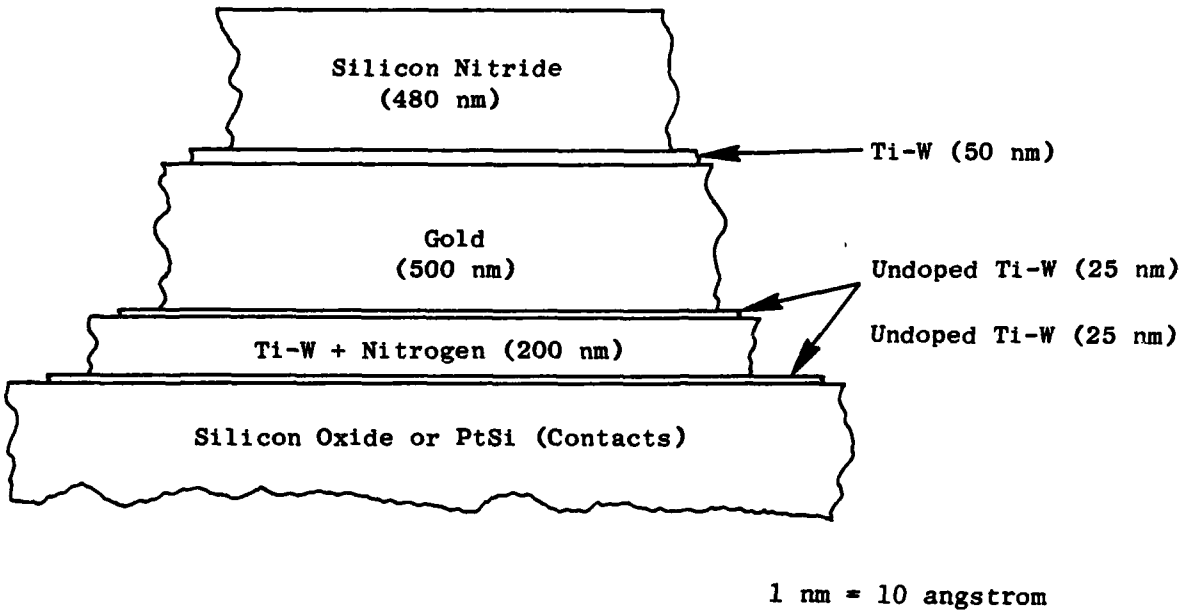


Figure 2. Structure of Multilayer Metal System.

Table 1. Life-Test Wafers and Probe Yield.

Wafer	Metallization	Yield
15	Normal Gold (Broken)	37% (28 Good Chips)
17	Normal Gold	29% (26 Good Chips)
19	Normal Gold	57% (51 Good Chips)
3	Hydrogen-Doped Gold	70% (62 Good Chips)
22	Hydrogen-Doped Gold	61% (55 Good Chips)
7	High-Temperature Gold	0%
13	High-Temperature Gold	Broken, Unfinished
16	High-Temperature Gold	0%

- Wafers with "hydrogen-doped gold" were sputtered with gold in the presence of a partial pressure of hydrogen.

The reasons for the complex layered structure and for the choice of these hree variations are detailed in Reference 2. In summary, the "normal gold" rocess established a baseline data point. The "high-temperature gold" deposi- ion process was intended to produce a stress-free condition at the elevated emperatures. (Differential thermal expansion introduces stress when the gold s deposited at ambient temperature.) The "hydrogen-doping" was an attempt to reclude gold-crystal formation by increasing intermolecular bonding.

The wafers were patterned using the E115 metallization mask. The normal old wafers and the hydrogen-doped gold wafers were patterned using a lift-off echnique. The high-temperature gold wafers were patterned by ion milling ecause the high-temperature deposition process was incompatible with the ift-off process. The patterned samples were covered with a 480-nm layer of ilicon nitride, and the bonding pad windows were opened by etching.

Eight wafers were processed: three with normal gold, three with hydrogen- loped gold, and two with high-temperature doped gold. Table 1 lists the wafers nd yields through wafer probe of the life-test circuits.

Both the normal gold and the hydrogen-doped gold samples had good yields, ut the high-temperature gold wafers all had zero yield. Measurements made sing the I^2L evaluation gates indicated that there was high electrical leak- ge in the devices. At first it was believed that the leakage was caused by damage which occurred during the ion-milling process. Previously, it had been bserved that leakage could be reduced by annealing the wafers for 30 minutes t 500° C. The wafers described above had not been annealed when first probed. ubsequent annealing did not increase yield or reduce leakage.

Two more wafers were metallized with high-temperature gold and annealed mmediately following ion milling. Probing indicated that there was gross leakage between the transistor elements. These wafers were examined in a scan- ning electron microscope (SEM) to search for the cause of the leakage. Resid- al metal was observed along the edges of oxide steps, and the leakage was robably due to this metal. Apparently, the ion milling had not been con- inued long enough to remove all of the metal from the vertical steps where he effective thickness of the metal is greater. Figure 3 is a SEM photograph howing the residual metal.

An attempt was made to remove the residual metal by chemical etching, but his resulted in undercutting of the gold. The one remaining undamaged wafer as then subjected to further ion milling after a new photoresist mask was pplied. After probing and SEM inspection indicated that the residual metal as gone, the wafer was annealed to remove ion-milling damage, and the life est circuits were probed. The yield was still zero. Further probing of the I^2L evaluation transistor indicated that the remaining problem was due to xcess contact resistance. Figure 4(a) is a curve tracer photograph of a ransistor showing the resistive nature of the contact. When a sufficiently large current is forced through the contact, the contact resistance is reduced,

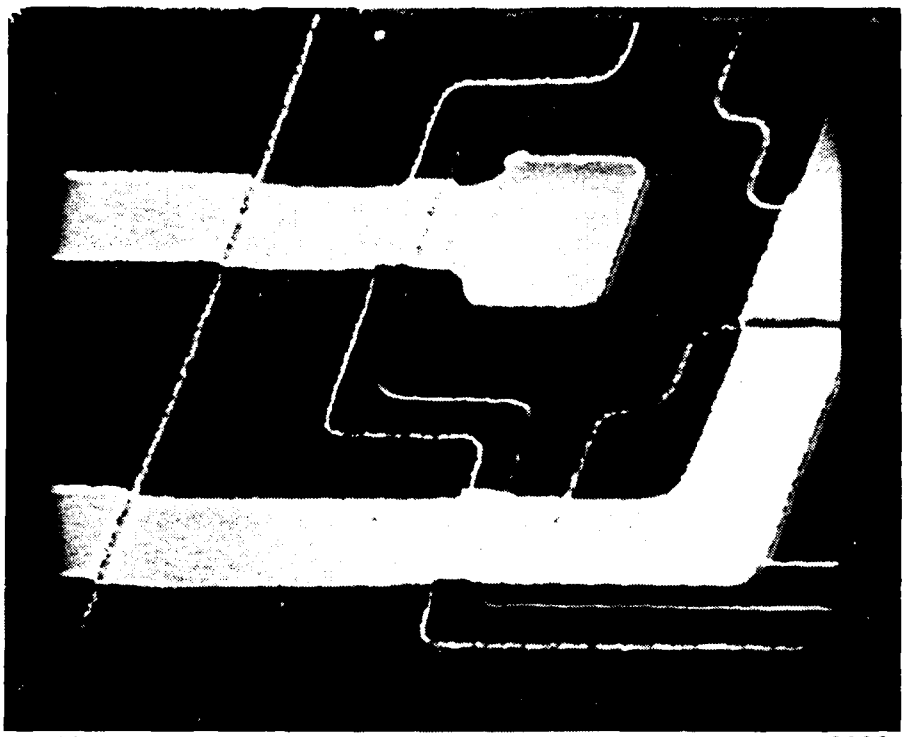
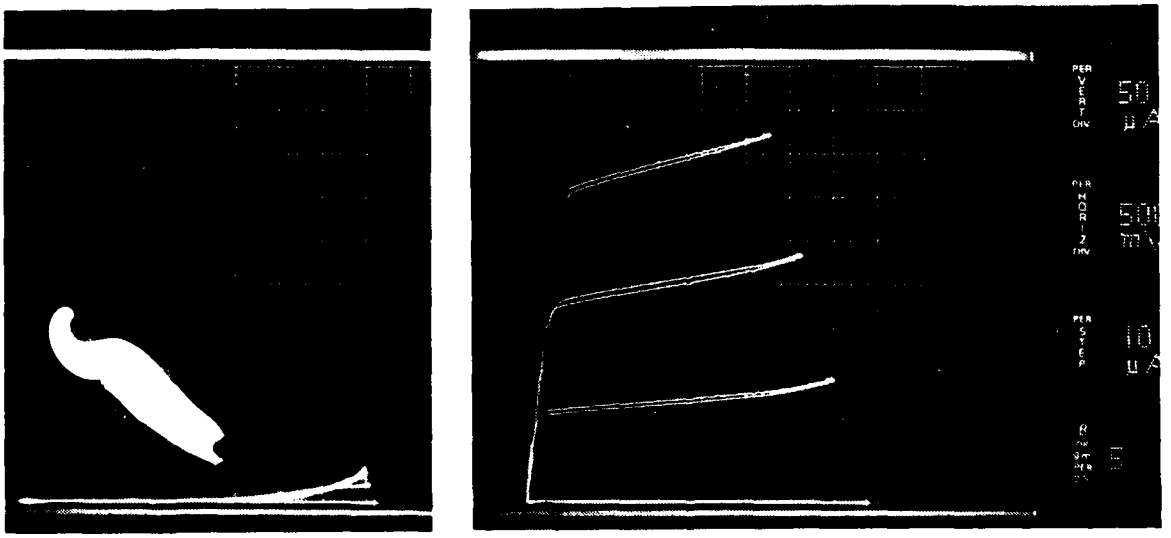


Figure 3. SEM Photograph Showing Residual Metal at Oxide Steps.



(a) Before Forcing Current (b) After Forcing Current

Figure 4. Curve - Tracer Photographs of Transistor Characteristic, Before and After Forcing Current, Indicative of Barrier Layer at Contact.

7.0 REFERENCES

1. Morris, W.L., et al., "High Temperature Electronics Technology, Phase I Final Report," General Electric Company, R80AEG212, March 1980.

2. Dening, D.C., "High Temperature Electronics Technology, Phase II Final Report," General Electric Company, R83AEB637, 1983.

6.0 DISCUSSION AND CONCLUSIONS

The results of this life test program are very encouraging. Microcircuits fabricated with a normal gold metallization system survived for over 2600 hours at 360° C without failure. This would be equivalent to over 18,000 hours at 300° C if a 1-eV activation energy were assumed. The actual activation energy for failure, if it exists, cannot be estimated since no valid failures occurred at either test temperature.

The normal gold system appears to be at least as reliable as the hydrogen-doped gold, based on the life test results. Analysis of the survivors indicated that the samples with hydrogen-doped gold had more of both crystal growths and voids. However, this may have been related more to the integrity of the nitride than to the nature of the gold. Differences may also have been more representative of wafer-to-wafer variations than of metallization variations.

The high-temperature metallization system evaluated in this program has been shown to be promising for use in high-temperature electronics. Further life testing for longer durations is recommended to verify that the voiding or crystal-growth mechanisms which have been observed do not represent ultimate causes of failure.

voids form in the 300° C samples only in the vicinity of crystal growths and near pad windows. Near the windows the compressive forces are relieved by gold diffusion into the window area. The gross voiding of the 360° C hydrogen-doped sample is not explained by this scenario. Optical inspection of this sample indicated that the nitride was perturbed, possibly lifting from the metal runs. Figure 17 is an optical photograph of Sample 22-9 showing this effect. Compressive stresses in the gold runs on this sample may have been relieved by lifting of the nitride, allowing the voids to form on cooling.

These phenomena, while interesting, have not been shown to cause failure in microcircuits. The crystal growths represent a potential failure mechanism for multilayer metal systems since they could cause shorting between adjacent metal runs or between the first and second layer. However, the crystal growths can be eliminated by using a thicker nitride layer or by ensuring that the nitride on the side walls of the runs is of high integrity. The positive results for the normal gold samples indicate that the latter is possible. Voiding does not appear to cause failure, and (if the postulated mechanism for void formation is valid) the void formation will not increase once the compressive stresses are relieved either by crystal growth or diffusion through window openings.

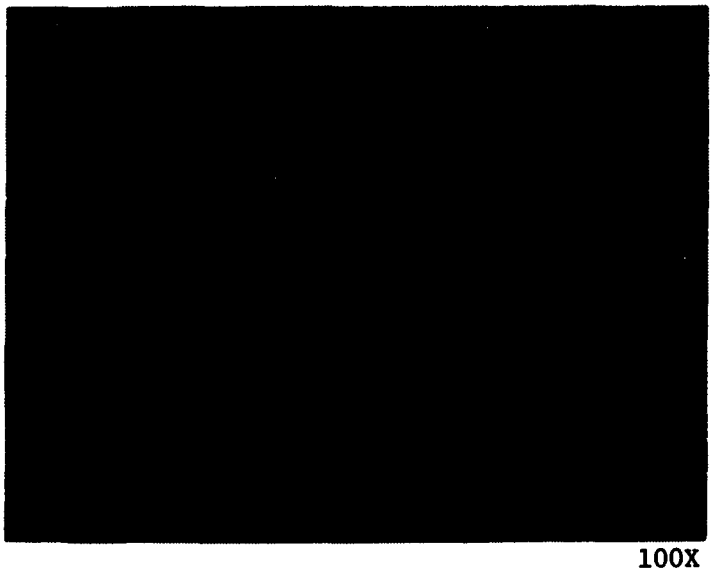


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Figure 17. Sample 22-9 (Hydrogen Doped) Showing Perturbations in Nitride Layer After 360° C Stress.

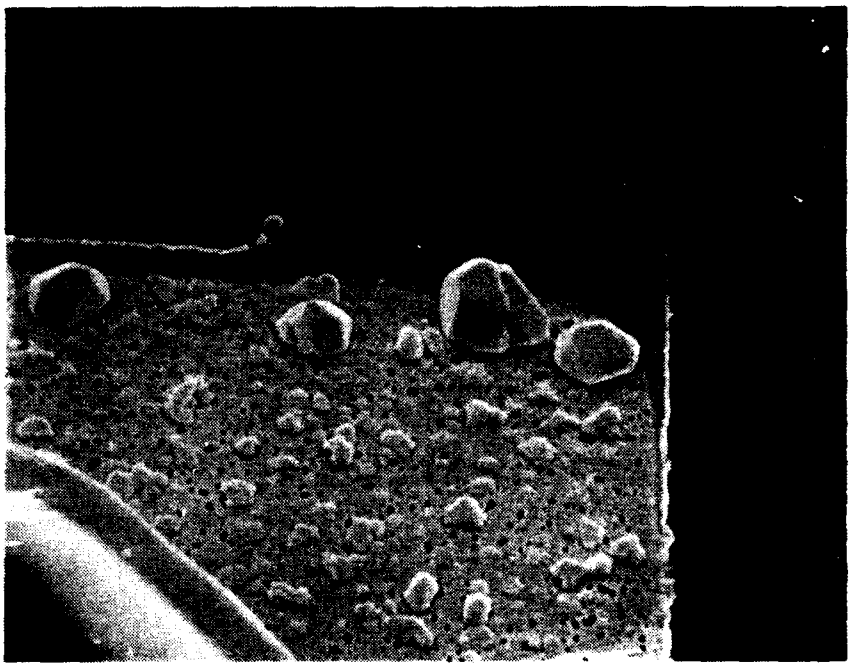

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Figure 16. Bond Pad Area on Sample 19-9 (Normal Gold Metallization) Showing Penetration of Voids into Run Area.

- In no case did crystal growths or voiding cause failure in the samples tested.

The crystal growths at the edges of the lines are known to be related to compressive stresses that build in the gold film when the sample is raised to the test temperature. (Both the silicon substrate and the nitride coating have a much smaller thermal expansion coefficient than the gold.) If the nitride coating on the edges of the metal lines is sufficiently weak it can crack, and the gold can be extruded or diffused through the crack, forming crystal growths, as observed. The greater tendency for the hydrogen-doped gold samples to form crystal growths may be related more to the relative thickness and integrity of the nitride on the two wafers than to the nature of the gold.

The formation of voids in the gold is more difficult to explain, particularly if the gold is in compression in the vicinity of the crystals. However, if it is assumed that the compressive forces developed in the gold as the temperature rises are relieved by the crystal growth in the vicinity of the crystals, the film will be put in tension as the sample cools. It is possible that the voids are formed during the cooling cycle. This would explain why

Figure 14. Bond Pad Area on Sample 22-9 (Hydrogen Doped).

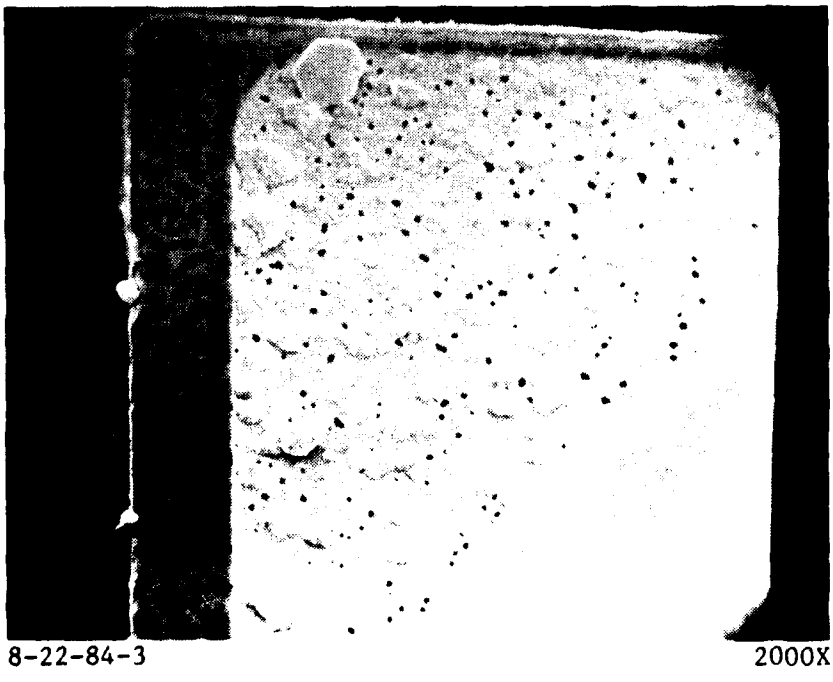

Figure 15. Bond Pad Area on Sample 19-9 (Normal Gold Metallization).

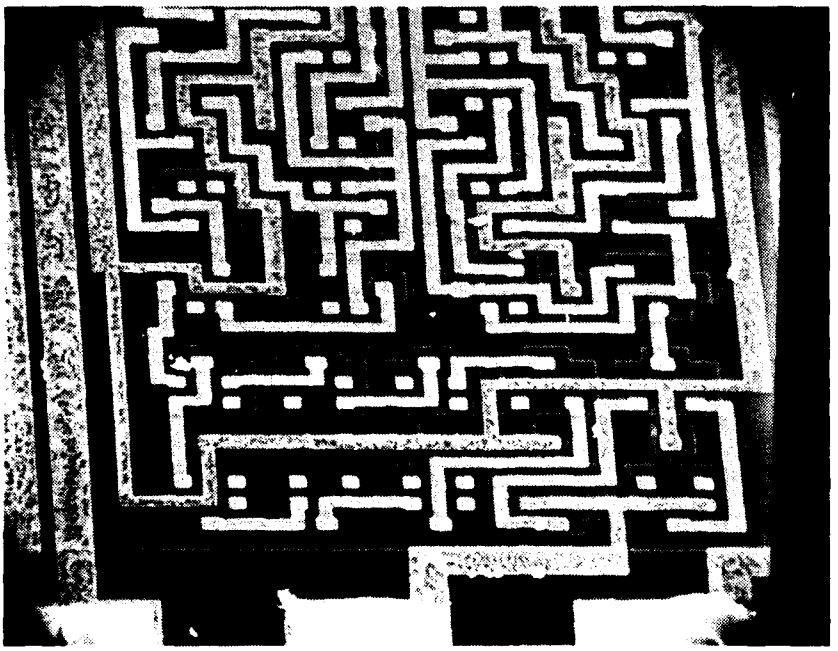

Figure 12. Gross Voiding on Sample 22-9 (Hydrogen Doped).

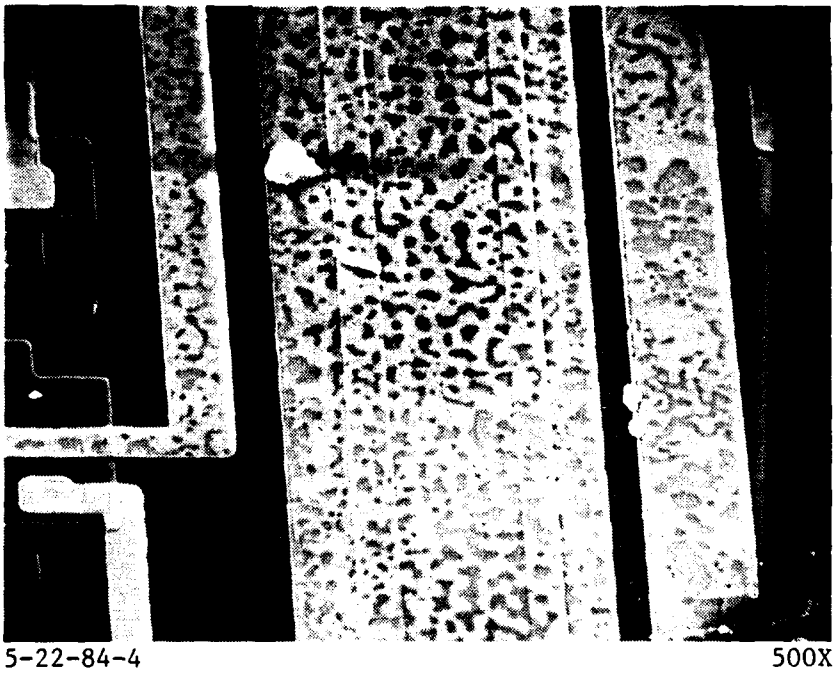

Figure 13. Closer View of Voiding in Sample 22-9.

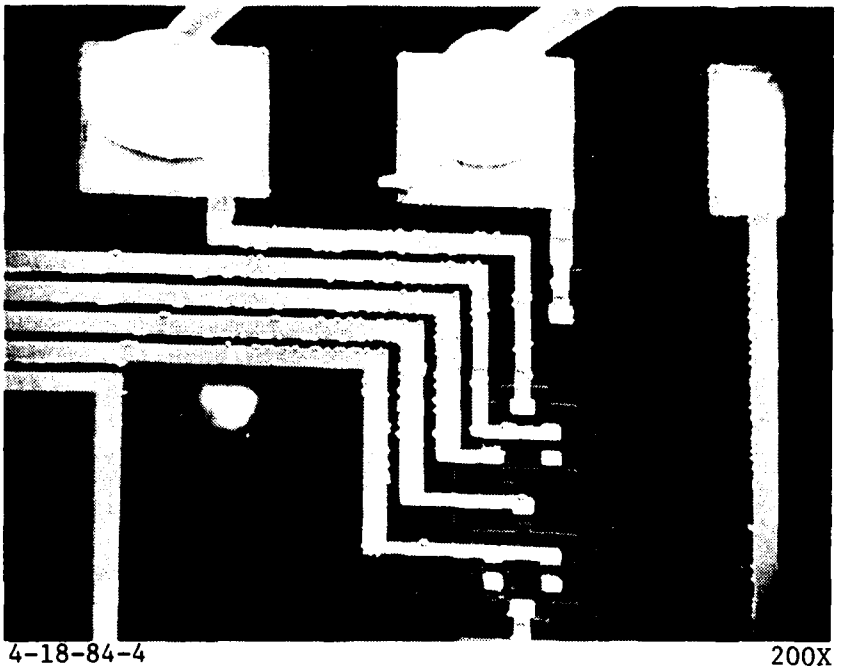

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Figure 10. Gold Crystal Growth on Sample 22-1 (Hydrogen Doped).

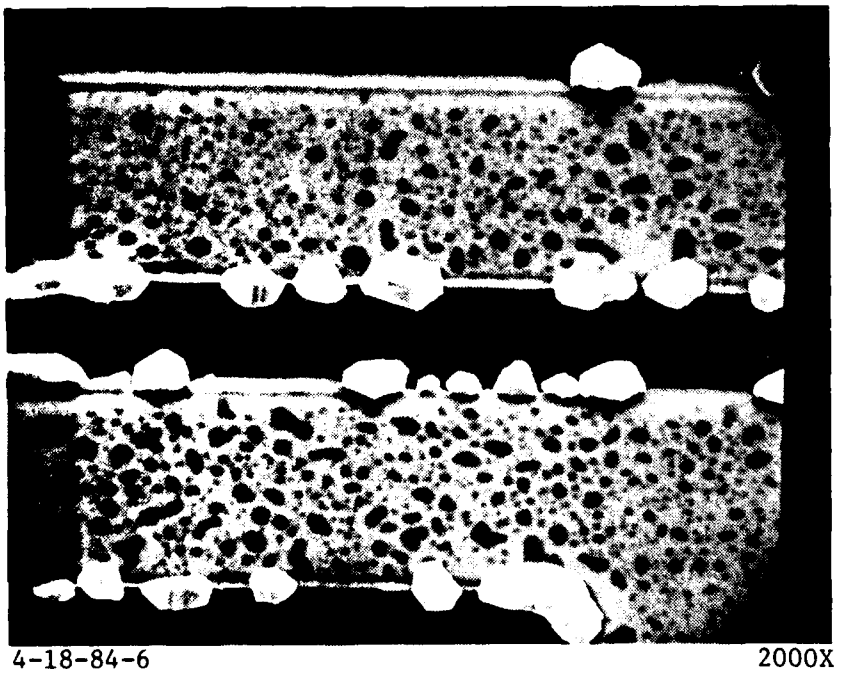

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Figure 11. Holes in Gold Runs Adjacent to Crystal Growth (Sample 22-1).

5.0 ANALYSIS OF STRESSED SAMPLES

The four packages removed from the 300° C life test after 2342 hours were opened and examined in the SEM for evidence of physical degradation. Subsequently, samples removed from the 360° C test were also examined. Several phenomena were noted. Gold crystals were found to be growing at the edges of the conductor lines, as shown in Figure 10. The density of crystal growth appears to be greater for the three hydrogen-doped samples than for the normal gold samples. Holes in the gold lines are also noted adjacent to the crystal growths. Figure 11 is a higher magnification view showing the crystals and the holes. The areas shown in these figures are of a portion of Sample 22-1, which was unpowered during the 300° C life test. Therefore, electromigration can be ruled out as a cause of the effects.

Figure 12 shows Sample 22-9, a hydrogen-doped sample which survived the 360° C life test. Gross voiding of the gold has occurred over many of the metal runs. Figure 13 is a closer view of some of these runs. Sample 19-9, a normal gold survivor of the 360° C life test, did not display this gross voiding.

Figure 14 shows a bonding pad area on Sample 22-9. Gross voiding of the gold occurs under the nitride around the periphery of the pad. Figure 15 shows the same phenomena for the normal gold sample, No. 19-9. The gold in the open area of the pad has also restructured, forming voids and nodules. Figure 16 is an SEM photograph of the area where a run joins a bonding pad on Sample 19-9. Voiding is restricted to the area immediately adjacent to the pad opening. This is not true for the hydrogen-doped sample, No. 22-9, as can be seen in Figure 12.

The above observations may be summarized as follows:

- Crystal growth at the edges of runs occurred for all samples examined.
- Crystal growths are much more prevalent in the hydrogen-doped samples than in the normal gold samples.
- Voiding of the gold runs occurred adjacent to the crystal growths and around the periphery of bonding pad windows on 300° C life-test samples with hydrogen-doped gold.
- Voiding was not evident on 300° C life-test samples with normal gold.
- Voiding occurred throughout 360° C life-test samples with hydrogen-doped gold.
- Voiding occurred only around the periphery of bonding pad windows on 360° C life-test samples with normal gold.

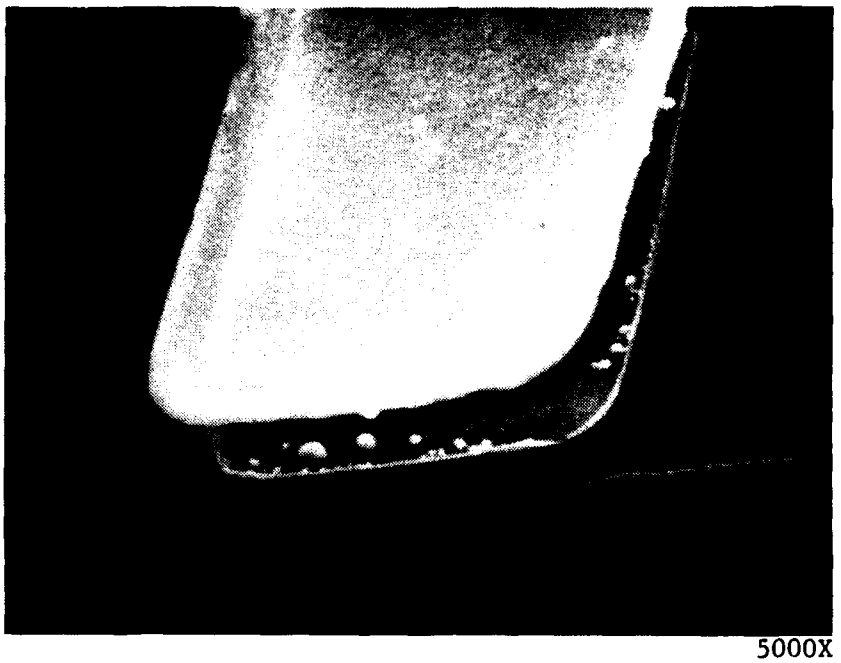

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Figure 8. SEM Photograph of Lifted Contact Pad on Failed Circuit.

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Figure 9. SEM Photograph of Area Where Nitride and Gold Had Lifted on Failed Circuit.

4.0 RESULTS OF LIFE TESTS

4.1 NONOPERATING LIFE TEST (360° C)

The 360° C life test was conducted for 2618 hours. Out of the 40 on test, 4 circuits failed. All four failures were on the same chip, indicating that the failures had a common cause, were defect related, and were not representative of the rest of the chips. The first three failures were observed after 1028 hours; the fourth occurred within 24 hours. There were no more failures during the subsequent 1590 hours of stress.

SEM analysis of the failed chip indicated that failure was due to lifting of the gold metallization at several locations. Figure 8 is an SEM photograph of a lifted contact pad. Figure 9 shows an area in which the nitride has lifted and the metal has lifted from the oxide. This figure also shows hillock growths along the edges of broad metal runs.

4.2 OPERATING LIFE TEST (300° C)

The 300° C life test was continued for 2342 hours with no failures out of 40 circuits being stressed. At that time, four packages were removed from stress: two each of the normal gold and the hydrogen-doped gold varieties. The remaining circuits were put back on stress for another 864 hours with no failures occurring. Therefore, 24 circuits withstood 3206 hours of stress without failure.

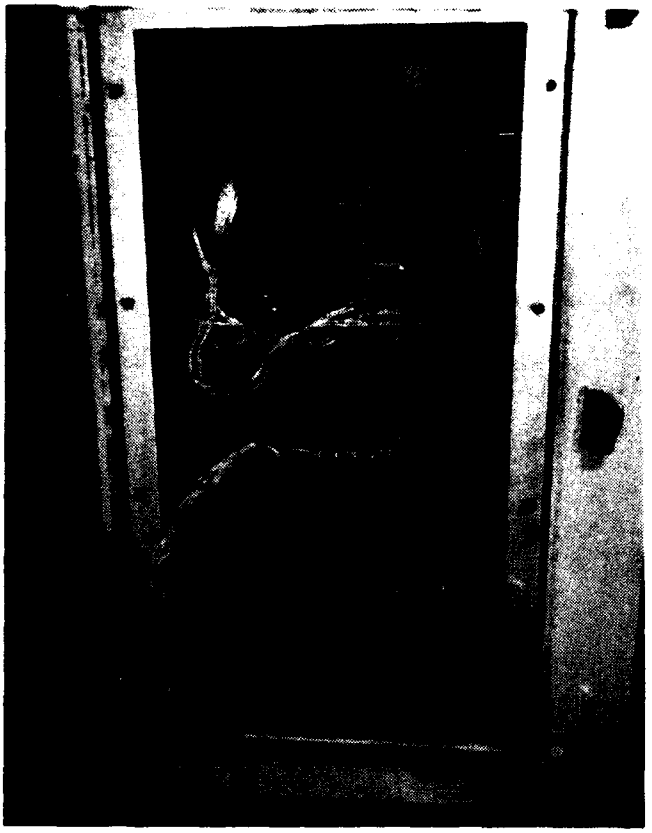


Figure 6. Operating-Life Test Boards in Oven.

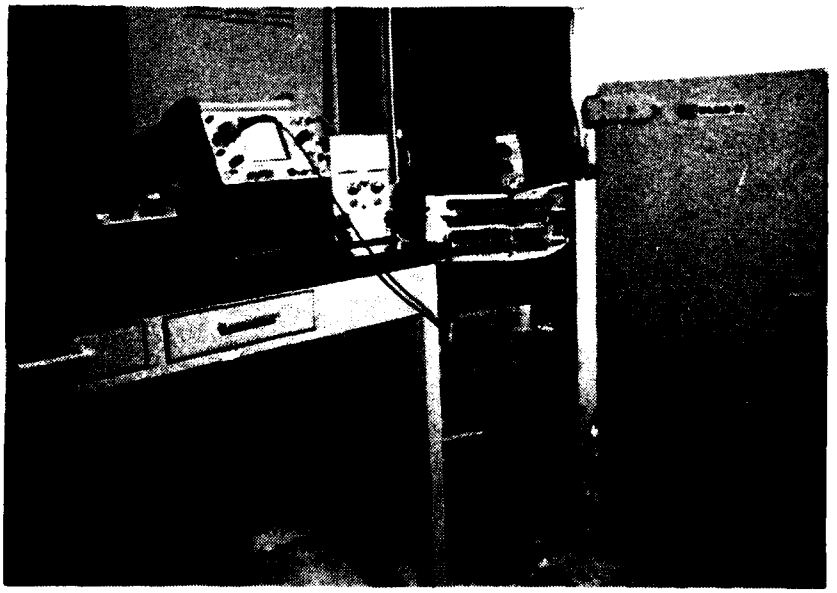
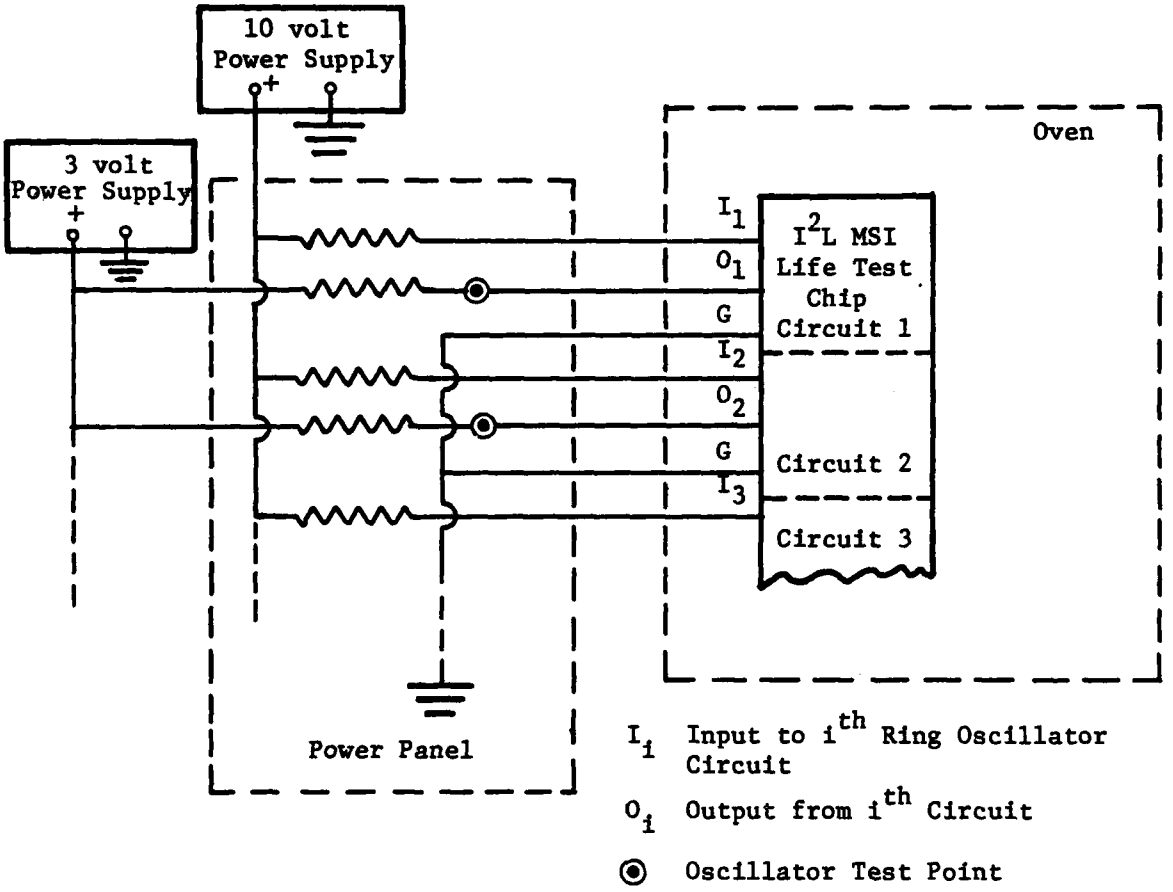
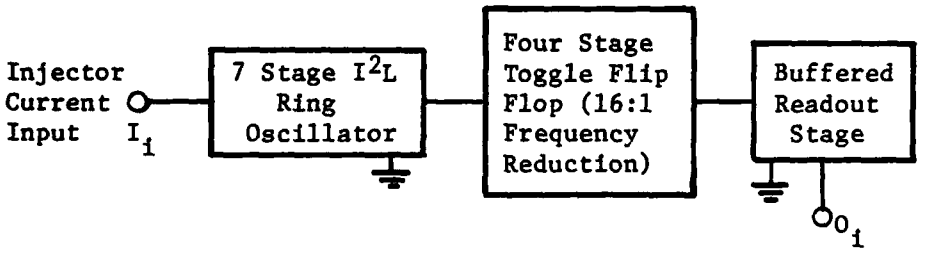


Figure 7. Overall-Life Test Setup.



(a) Schematic Wiring Layout



(b) Block Diagram Schematic

Figure 5. Schematic of Operating-Life Test Circuit.

3.0 DESCRIPTION OF LIFE TESTS

Two life tests were conducted: an operating-life test at 300° C and a nonoperating-life test at 360° C. Ten packages were placed on test at each temperature, five of each metal variation. Since each package contained a chip with four MSI test circuits on it, a total of 20 circuits with each metal variation were tested at each temperature.

3.1 NONOPERATING LIFE TEST (360° C)

The ten packages were placed in a diffusion furnace in a nitrogen atmosphere at 360° C and were removed periodically for an electrical functional test at room temperature.

3.2 OPERATING LIFE TEST (300° C)

Figure 5 is a schematic of the test circuit used for the operating-life test. The injector is supplied with 10 mA, and the output is connected to a 3-V supply through a 2.2-kΩ resistor. An oscilloscope monitors the output signal at the test points shown.

The packages are mounted in high-temperature sockets clamped to aluminum boards. Nickel ribbon is welded to the socket terminals and connects the terminals to binding posts mounted on the aluminum board with ceramic standoffs. High-temperature wire is used to connect the binding posts to a power panel mounted outside the oven. The power panel contains the biasing resistors and facilitates probing of the individual test-circuit outputs. Figure 6 is a photograph of the test board in the oven, and Figure 7 shows the overall test facility.

The test procedure is as follows. The packages are mounted in the oven at room temperature, and all circuits are checked for operation by monitoring the test point with the oscilloscope. The temperature of the oven is allowed to rise to 300° C, and the operation of the circuits is monitored during the rise. Most circuits stopped oscillating above about 275° C. The biasing was maintained at 300° C; periodically the temperature was reduced to 275° C and the circuits were monitored to see if they still oscillated. The amplitude of the oscillations was measured for each circuit by recording the voltage at the test point using a d.c. voltmeter.

as shown in Figure 4(b). This contact problem is associated with the platinum silicide formation process and may be due to a very thin residual oxide on the silicon which prevented PtSi formation.

Because this problem could not be eliminated by further processing, further attempts to fabricate and test high-temperature gold samples were discontinued.

2.3 PACKAGING

Wafers 19 and 22 were selected for packaging. As shown in Table 1, the former was a normal gold wafer, and the latter was a hydrogen-doped gold wafer. After the wafers had been cut, they were visually inspected and the (cosmetically good) dies were selected for packaging. The chips were mounted in 24-pin ceramic dips, and ceramic lids were sealed on using glass frit. Tests indicated that the packages were hermetic after sealing. Electrical testing of the packaged circuits yielded the following:

Wafer 19: 21 good, 7 low gain, 1 bad

Wafer 22: 17 good, 4 bad.

APPENDIX

RELIABILITY OF HIGH-TEMPERATURE I^2L CIRCUITS

This appendix is a reprint of a technical paper presented at the International Reliability Physics Symposium held at Las Vegas, Nevada in April 1984.

RELIABILITY OF HIGH TEMPERATURE I^2L INTEGRATED CIRCUITS

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I. SUMMARY

Silicon based I^2L circuits have survived a life test for over 5000 hours at 340°C without degradation. These chips used aluminum metallization with current densities below 10,000 amp/sq.cm to avoid electromigration failures. The need for a gold based metal system for high temperature applications has lead to the development of Ti-W diffusion barriers which have withstood temperatures of 360°C for longer than 3500 hours without change. MSI integrated circuits with a Ti-W/Au metallization system have withstood stress tests of over 2000 hours at 360°C. Gold hillock formation has been shown to be caused by the compressive strains induced in the gold film by thermal expansion mismatches. The driving force for gold hillock formation may be eliminated by depositing the gold film at elevated temperatures.

II. INTRODUCTION

Integrated circuits capable of operating for long periods of time at temperatures as high as 300°C are necessary for several high temperature electronics applications, including aircraft engine controls and geothermal well electronics. Most currently available microcircuits are specified to operate at temperatures no higher than 125°C. This paper describes the status of a program to develop microcircuits which can operate reliably at temperatures as high as 300°C.

Early in the program, an evaluation of various microcircuit technologies was conducted to determine which technologies have the capability of operating at these high temperatures. It was found that many existing microcircuits can continue to function at temperatures above 300°C but that I^2L, CMOS/SOS, and dielectrically isolated technologies offered the most promise of supporting a full family of circuit functions. The I^2L technology was chosen for further development since the General Electric Company had a radiation hardened I^2L technology which operated at temperatures in excess of 300°C.

This paper describes the failure mechanisms which have been found to limit high temperature life and the approaches taken in reducing susceptibility to these mechanisms in order to attain adequate circuit lifetimes. The mechanisms associated with the silicon are considered first, followed by a discussion of the mechanisms associated with the metallization system. During this discussion, the evolution of the technology to its present status and the reasons for choosing the present structure are made clear. The results of life testing of MSI circuits fabricated using the new technology are presented.

III. BIPOLAR SILICON RELIABILITY

For this investigation the sources of failure for the high temperature integrated circuits have been divided into: mechanisms affecting the silicon devices and those affecting the metallization and connections to the external world. No problems have been experienced during this program with failures of bipolar silicon semiconductors due to thermal stresses. The processing induced changes during the fabrication cycle (diffusions and oxidations) occur at temperatures around 900°C to 1050°C. The reaction rates for the continuation of such processes at temperatures around 300°C are slow enough that they will not be a factor within the lifetime goals.

The long term reliability of CMOS/SOS or dielectrically isolated CMOS was not investigated. The potential for surface state instabilities that could cause threshold shifts was of concern. An I^2L technology with its active regions buried inside the silicon was judged to be more stable than a field effect based approach.

Life tests were conducted to verify the suspected endurance of bipolar silicon based integrated circuits and to evaluate any failure modes of I^2L devices under high temperature stress. The circuits in this test used an aluminum metallization in which the current densities were kept below 10,000 amp/sq cm to avoid electromigration induced failures. Accelerated life tests were run at two temperatures, 340°C and 360°C, with ten samples tested at each temperature. Each sample contained three ring oscillators, for a total of thirty oscillators tested at each temperature.

The 340°C test was conducted in an oven with the circuits powered at 30 μA/gate. The oven temperature was lowered to 250°C for functional verification since the oscillators would not operate at the test temperature with the applied injection current. The 360° C test was conducted in a diffusion furnace with the chips unpowered. The chips in the 360°C test were removed and cooled to room temperature for operational tests.

Table I summarizes results. The 340°C test was terminated after 5086 hours so that the oven could be used for other life tests. Circuits that were examined at the conclusion of that test were unchanged from samples that had not been subjected to the test, as

TABLE I. Accelerated Life Test Results for Bipolar I^2L

340°C Powered Test		360°C Unpowered Test	
Hours	No. Failed	Hours	No. Failed
0	0	0	0
21	0	25	0
69	0	71	0
134	0	165	0
302	0	235	0
376	0	401	0
828	0	568	0
968	0	813	0
1589	0	1333	0
2269	0	1668	0
3244	0	2269	0
3725	0	3177	0
4584	0	3848	0
5086	0	4589	0
		5285	0
		5981	1
		6430	1
		6770	1
		7874	2

CH1990-1/84/0000-0030$1.00 1984 IEEE/IRPS

shown in Figure 1. The unpowered stress test at 360°C is continuing. At 2269 hours in the 360°C test all three oscillators in one package were observed to operate at reduced amplitude. This was not counted as a failure since the silicon devices were obviously still functioning and no further change has been observed. The first failure occurred at the 5981 hour point when an oscillator (in a different package) could not be made to operate.

The powered life test was designed so that the metallization would not be stressed to failure since silicon failures could not then be detected. While this life test demonstrates that there do not appear to be any bulk related mechanisms that would limit the life of the silicon bipolar devices at temperatures less that 360°C, the current densities employed in the metallization runs are low compared to present LSI circuit design practices.

IV. GOLD BASED, HIGH TEMPERATURE METALLIZATION

A gold based metallization system for high temperature integrated circuits is desired for: improved resistance to electromigration, the convenience that gold provides in packaging, the lower resistivity that can be obtained compared to silicides or refractory metallizations and, compatibility with "the external world" for hybrid applications. This approach to the metallization does introduce problems with interdiffusion between the gold and the silicon semiconductor. A stable diffusion barrier is needed between the gold and silicon which is compatible with the total integrated circuit fabrication cycle.

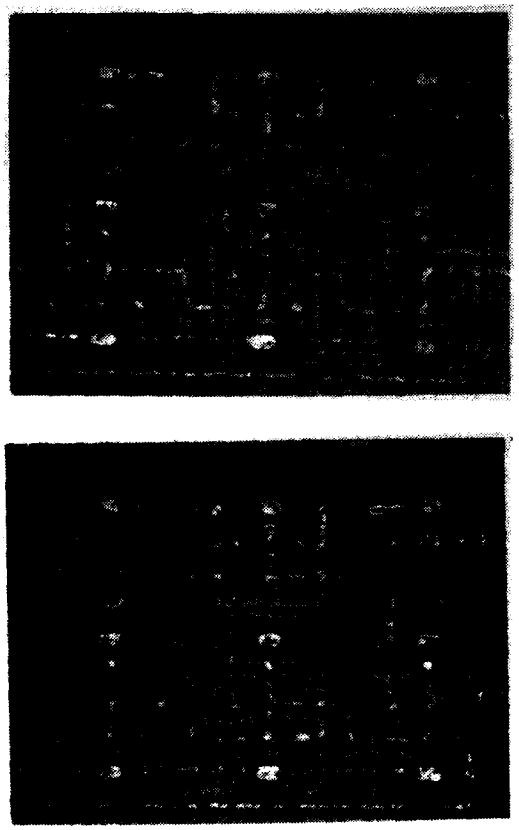


Fig. 1 Comparison of an aluminum metallized integrated circuit after 5086 hours at 340°C (top) and an untested sample (bottom).

Ti-W was chosen as a preliminary diffusion barrier since it is a commonly used barrier with gold metallizations. A diffusion barrier of "as sputtered" Ti-W was found to fail after times as short as 100 hours at 350°C (see Figure 2). Without an effective barrier the silicon semiconductor material and the gold metallization can interdiffuse as shown in Figure 3. Silicon dissolving into the gold would be supplied from the device contact regions. Gold dissolving into the silicon in the contact regions can leave voids and open circuits in the interconnect lines. Finally, gold doping in the silicon will shorten minority carrier lifetimes and cause transistor gains to degrade.

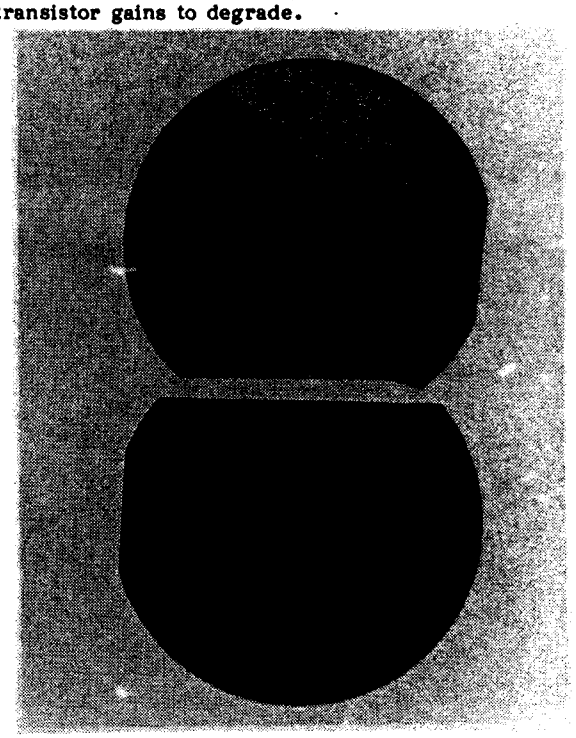
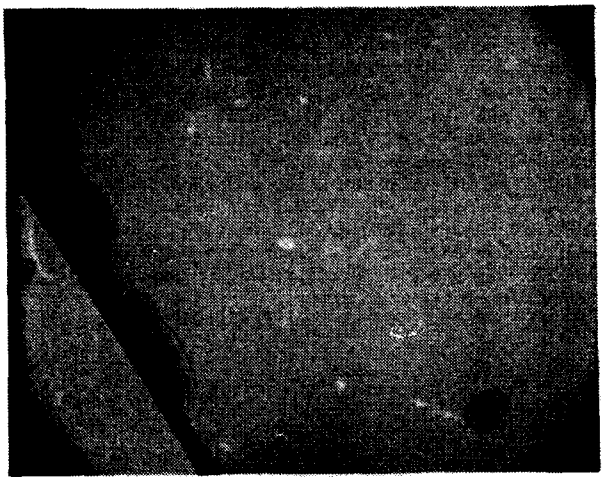


Fig. 2 Evaluation of undoped Ti-W diffusion barriers for separating gold and silicon. Both samples have been annealed for 100 hours at 350°C in nitrogen.

The addition of a nitrogen "stuffing"[1] to the Ti-W layer transforms it into an excellent diffusion barrier. The nitrogen doping was introduced into the Ti-W diffusion barrier during the sputtering process by mixing about 10% nitrogen to the argon atmosphere inside the chamber. The nitrogen doped diffusion barrier provides good protection against the interdiffusion of silicon and the gold metallization but the nitrogen doping changed the adhesion properties of the Ti-W barrier layer. Tape tests and pull tests indicated that the adhesion between the Ti-W and the wafer oxide and between the Ti-W and the gold layer were about 1000 psi in "nitrogen stuffed" samples. Failures in life tests due to lifting metal lines, shown in Figure 4, and problems during the bonding operation of chip packaging, as shown in Figure 5, were attributed to reduced adhesion resulting from the nitrogen doping in the diffusion barrier. The addition of an undoped Ti-W layer on the top and bottom of the nitrogen doped layer restored the adhesion level to greater than 8000 psi.

Thin film test structures were deposited during the processing of the life test samples. The test films consisted of nitrogen doped Ti-W on PtSi, followed by a gold top layer. After deposition, half of a sample wafer was annealed in a 360°C diffusion furnace for



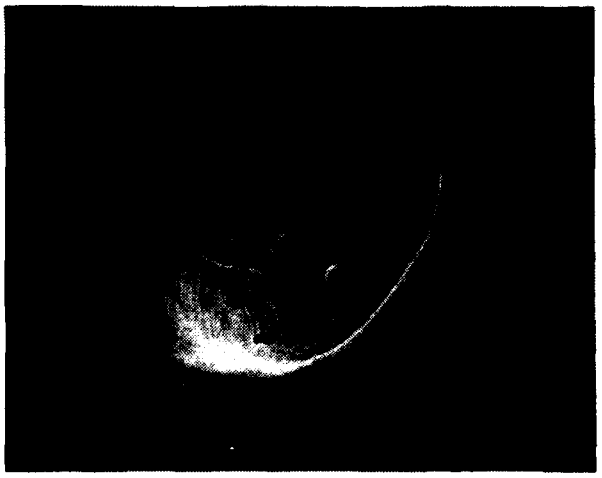


Fig. 3 Gold migration through a point defect in the Ti-W diffusion barrier is revealed after annealing for 100 hours at 365°C. The top photograph shows the defect and the edge of a 2 inch wafer at 10X. A close-up of the defect and the ring structure caused by silicon migration into the gold film is shown in the middle photograph at 100X. Finally, the bottom photograph at 1000X shows the depression in the gold film left by the diffusion of the gold into the silicon substrate and the barrier defect in the center of the pit.

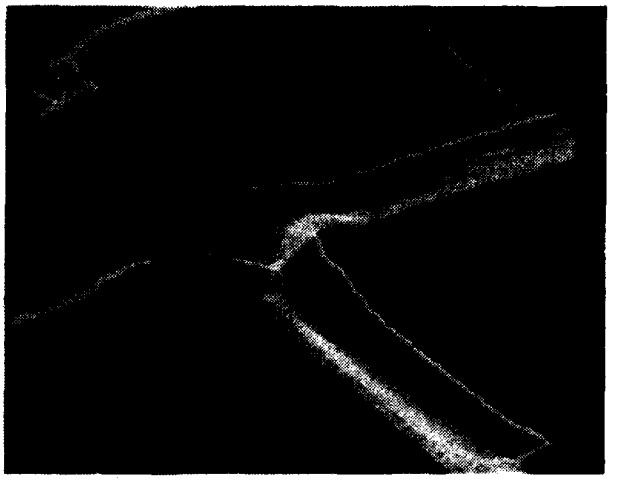


Fig. 4 This loss of adhesion between the Ti-W layer and the integrated circuit field oxide was observed after 1220 hours at 340°C.

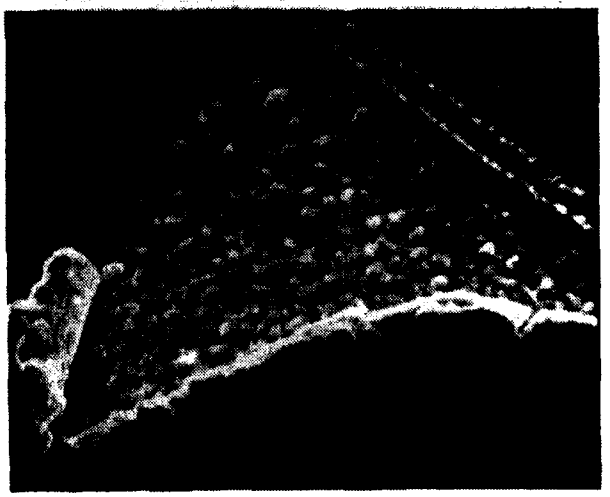


Fig. 5 A heavily nitrogen doped Ti-W diffusion barrier caused the reduction in adhesion between itself and the top gold layer. The reduced adhesion was discovered at the bonding operation as shown in the top photograph. The bottom photograph shows a close-up of the corner bonding pad with the gold lifting from the Ti-W layer.

over 3500 hours while the other half was stored at room temperature. An Auger profile of the as deposited structure is shown in Figure 6. A well defined nitrogen doped Ti-W diffusion barrier is shown. Some oxygen at the Au/Ti-W interface is observed due to the gettering action of Ti-W. After annealing, the degree of interdiffusion increased, as shown in the Auger profile in Figure 7. In particular, the tungsten and titanium have penetrated into the bulk of the gold film and have moved into the silicon. There is some indication of a pending barrier breakdown since the gold and silicon are in close proximity of each other after annealing. However, the diffusion barrier remains effective even though metal migration occurs during the anneal process. Tests indicate that lifetimes will exceed the desired goal for any reasonably expected acceleration factors.

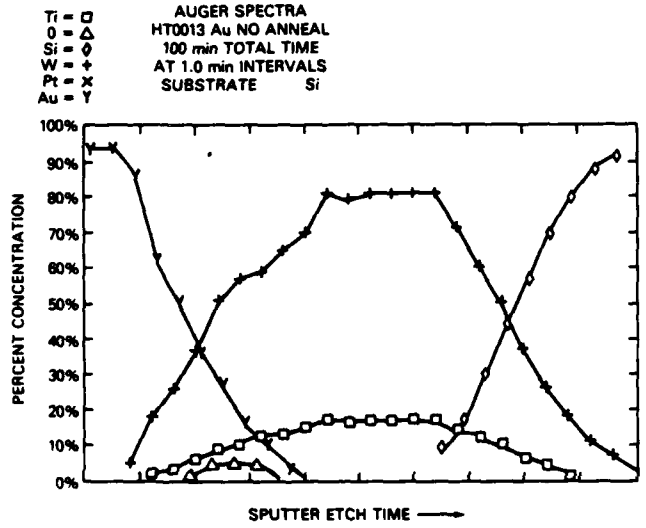


Fig. 6 The Auger profile of the as deposited metallization system shows the abrupt interfaces between the layers.

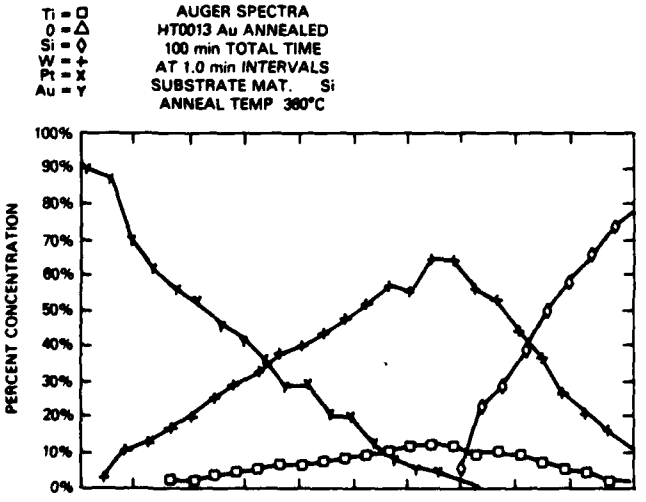


Fig. 7 The Auger spectra profile of the sample after annealing for over 3500 hours at 360°C shows some movement in the Ti-W layer.

One of the discoveries in the failure analysis of the initial life test samples was the presence of hillocks and voids in the unpassivated metallization layers [2]. Single crystals were observed growing from the top and sides of the metal runs (see Figure 8). SEM microprobe analysis of the crystals indicated that they were composed of pure gold within the limits of the measurements.

The cause of the gold crystal growth was hypothesized to be due to the thermal expansion mismatch between the gold film and the silicon wafer substrate. At some elevated temperature the gold film would be placed in compression since gold expands more rapidly than silicon. The compressive force on the gold provides the driving force for crystal growth as gold atoms migrated to regions of lower potential energy. This movement is aided by the increased mobility of gold atoms at elevated temperatures.

A wafer stress fixture was constructed to verify the crystal growth hypothesis by mechanically providing strain in the gold layer. The fixture was designed to support a wafer around its circumference and to deflect the wafer center with a screw (40 threads per inch) to provide the strain. To calibrate the fixture, a Ti-W/Au metallized 3" wafer was fitted with strain gauges and placed in the fixture. Strain measurements were made at room temperature and in a 66°C oven (the maximum temperature limit for the strain gauges). The strain profile did not change when the fixture was placed in the oven, indicating that the strain induced by the fixture did not change with temperature.

The interface strain due to the thermal expansion mismatch between Ti-W and Au was estimated to be on the order of 2500 μin/in at 350°C assuming that there was zero strain at 100°C. The maximum strain that could be safely produced by the fixture without wafer breakage was about one sixth of that value. As a result, an annealing experiment could not be implemented that completely canceled the thermal strain with mechanical strain. The strain fixture was used to modulate the thermal induced strain by adding and subtracting the mechanical strain.

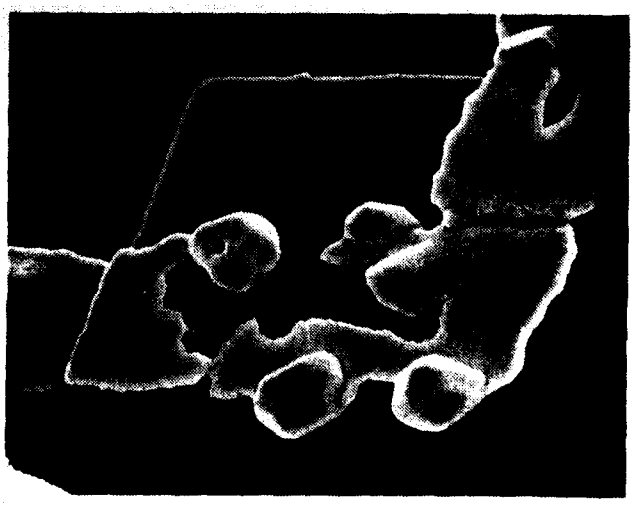


Fig. 8 Hillock and void formation caused failures in the initial unpassivated metallization. The sample shown above failed after 320 hours at 320°C.

Two 3" silicon wafers with Ti-W/Au metallization were annealed at 350°C for 347 hours. One wafer had the force applied to the gold side (gold under mechanical compression) and one with the force applied to the silicon side (gold under mechanical tension). Both wafers had one full turn of the screw which would produce a strain of approximately 400 μin/in at the wafer center. After annealing the wafers, the gold under the highest compressive strain showed the formation of larger gold crystals than the wafer with the gold under "tension". Figure 9 shows photographs of similar regions of both wafers. A strong correlation between the stress inside the gold film and hillock growth can be seen from this non quantitative experiment. The crystal density also changed radially across the wafer, tracking the applied strain.

The failure rate due to gold hillock growth may be reduced by suppressing hillock formation. This has been attempted in two ways. First, the driving force can be eliminated by depositing the gold at high temperatures [2]. Second, a passivation layer can be deposited to constrain the metallization surface and prevent hillock growth.

If a thermal expansion mismatch is the cause of the crystal growth in the gold metal layer when they are annealed at high temperatures then an obvious solution is to deposit the metallization onto wafers that are heated to this temperature range. Then there would be no induced stains in films at the elevated temperature while at all lower temperatures the strain on the gold would be tensile and not conducive to crystal formation.

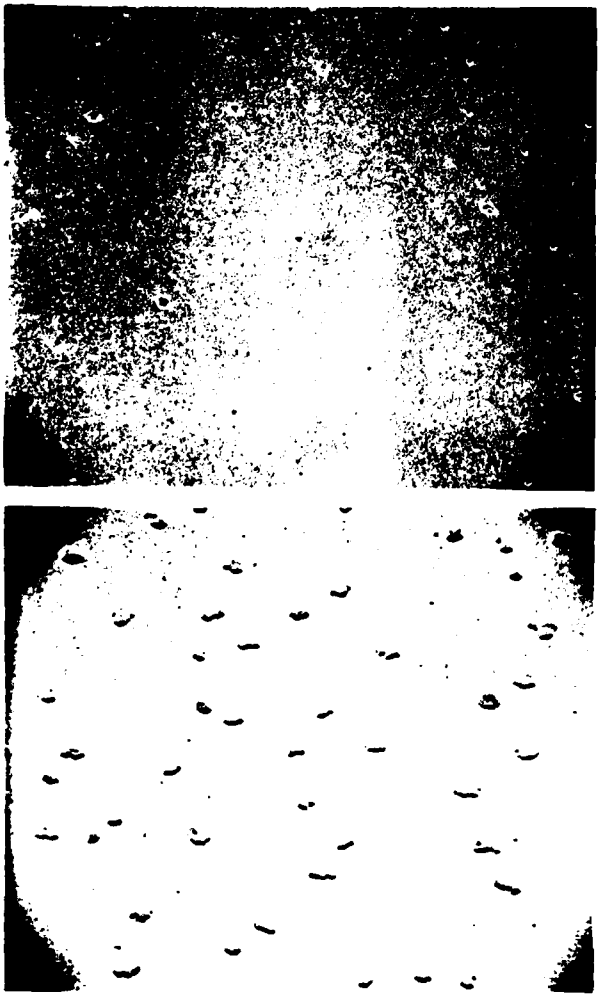


Fig. 9 Gold hillock formation is reduced in Ti-W/Au films when the films are annealed while the gold is in tension (top) as compared to annealing with the gold in mechanical compression (bottom).

Passivation layers have been shown to reduce hillock formation in integrated circuit metallizations as can be seen in Figure 10. For this approach to be successful the passivation layer must adhere to the metal layer and maintain its integrity during extended periods at high temperatures. A thin (500 Å) layer of undoped Ti-W was deposited on top of the metallization to enhance the adhesion between the gold and the passivation. To minimize cracking in the passivation the deposition parameters were adjusted to form a silicon nitride layer with an internal compressive stress.

V. LIFE TEST OF THE COMPLETE SYSTEM

A life test was conducted to demonstrate the effect of the improvements in the metallization system. A special life test circuit was constructed with 50 I^2L logic gates. The circuit consisted of a seven stage ring oscillator providing clock signals to a four bit binary counter. This MSI level of complexity circuit was replicated four times on each chip to form the life test component shown in Figure 11. The advantage of such a circuit for a life test is that the function is self testing with only three connections (power, ground, and output signal) needed to be brought outside the oven.

To prepare samples for life testing, silicon wafers were diffused with the gate patterns and PtSi was formed in the device contacts. The metallization was deposited and patterned with a lift-off technique followed by the deposition of a passivation layer. The metallization/passivation system that was applied to the life test samples is shown in Figure 12.

The life test set up is shown in Figure 13. The microcircuits were mounted in an oven on the high temperature test boards, shown in Figure 14. Each board consists of an aluminum framework to which high temperature sockets are clamped. Connections to the sockets are made by welding nickel ribbon to the socket pins and connecting the other ends of the

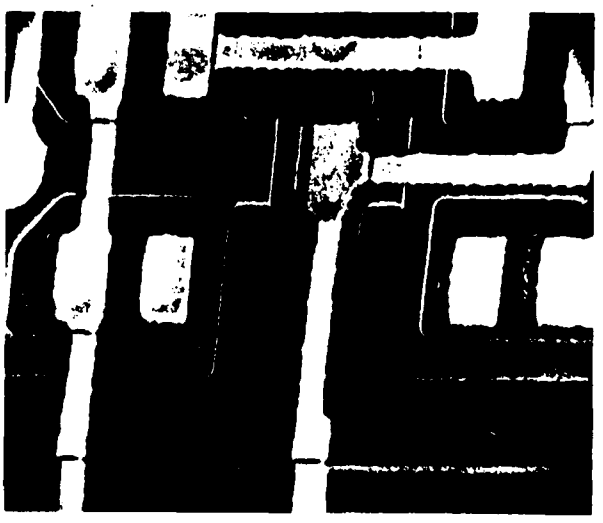


Fig. 10 The deposition of a silicon nitride passivation layer can suppress hillock formation as long as its integrity is maintained. This sample has endured 509 hours at 360°C without hillock formation.

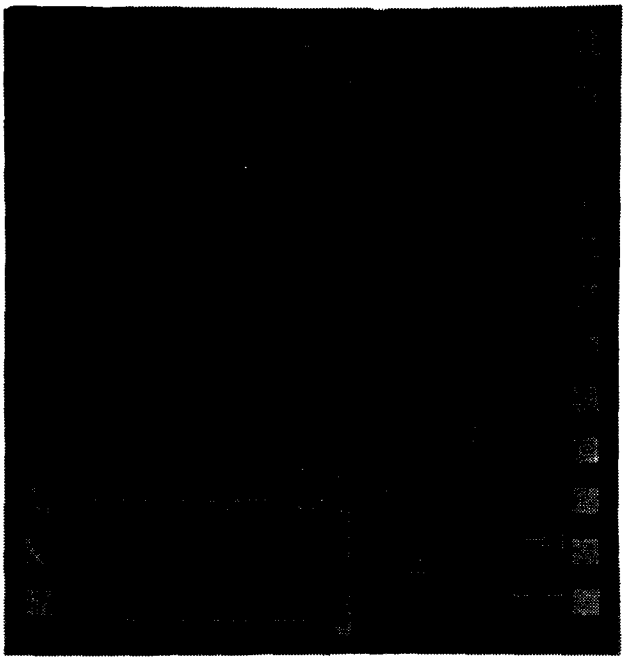


Fig. 11 Four MSI level of complexity digital circuits were incorporated in the circuit for life testing as shown in this microphotograph of the chip.

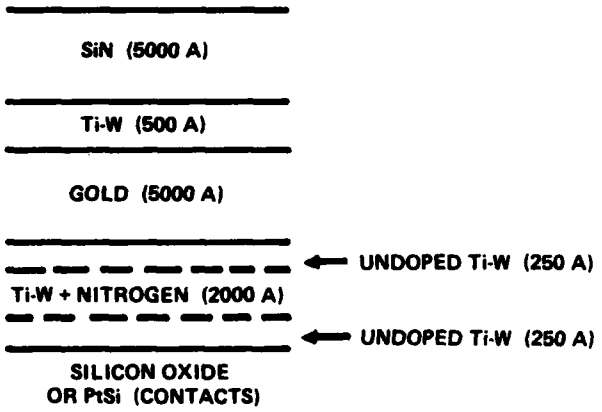


Fig. 12 The high temperature integrated circuit metallization system as shown above is deposited without breaking vacuum. The interconnect lines were defined followed by the deposition of the silicon nitride passivation layer.

ribbon to ceramic stand-offs attached to the board. The boards are connected to the external test circuit using high temperature wire. During the test, both the input currents and the output waveform are monitored. Some of the ring oscillator/counter test elements stop oscillating at temperatures above 275°C and in order to check the circuits for operation the temperature is temporarily lowered to 275 °C and then returned to 300°C to continue the test.

After 2000 hours of testing at 300°C there have been no failures out of 10 packages containing 40 ring oscillator/counter test elements.

An unpowered life test was conducted in a diffusion furnace set at 360°C. The packaged circuits were removed from the furnace and cooled to room temperature for evaluation. A total of ten chip packages were used with each sample containing four of the MSI life test circuits for a total of forty circuits on test. The results of this test are shown below in Table II.

TABLE II. Unpowered Life Test at 360°C

Hours	Number Failed
0	0
168	0
336	0
667	0
1028	3
1467	4
2114	4

All four of the failed oscillator/counter circuits were in the same package, indicating that these failures were anomalous. Failure analysis indicated that failure was due to loss of metal and oxide adhesion.

Fig. 13 300°C powered testing is performed in this life test facility.

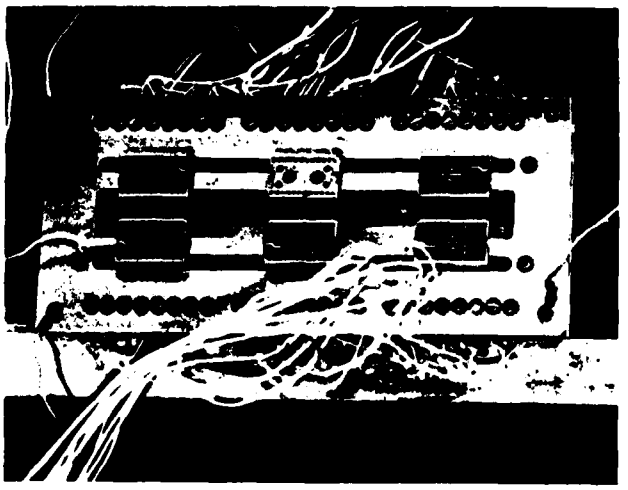


Fig. 14 Aluminum boards with high temperature sockets interconnected with welded nickel ribbon were used for the 300°C operating life test.

VI. DISCUSSION

We have shown that the high temperature life of an I^2L integrated circuit is not limited by degradation of the silicon itself, but rather by the degradation of the metallization system or by the interaction between the metallization and the silicon. In particular aluminum metallization is limited both by electromigration and by its interaction with silicon [3]. A gold metallization system with a metallurgical barrier was chosen for this work because of its lower susceptibility to electromigration.

The conventional Ti-W/Au system was found to be inadequate at temperatures above 300°C for two basic reasons: the Ti-W was not an effective barrier to gold penetration at these temperatures, and rapid gold hillock formation occurred due to residual strains in the gold film. An adequate barrier was achieved by "stuffing" the Ti-W layer with nitrogen and the gold hillocks were suppressed by depositing the gold at elevated temperatures. Since the "stuffing" adversely affected the adhesion of the Ti-W to both the gold and the silicon oxide a more complex layered system has been evolved to solve these problems. The results of life tests carried out to evaluate this multilayered metallization system are encouraging. MSI circuits have operated for over 2000 hours at 300°C without failure.

The acceleration factors for life testing at 360°C as compared to the 300°C temperature goal are not known since the activation energies for failure modes have not been determined. If the activation energies fall in the range from .6 to 1.0 eV then acceleration factors between 3.2 and 6.8 may be expected. Failures due to changes in the metallization system are expected to be the ultimate lifetime limiting phenomenon.

VII. CONCLUSIONS

- IIL integrated circuits with Al metallization can operate reliably at 300°C for over 7000 hours if current densities are low.

- Life tests of MSI microcircuits fabricated using Ti-W/Au metallizations have demonstrated lifetimes exceeding 2000 hours at 360°C.

- A nitrogen doped Ti-W Diffusion Barriers has been shown to be an effective diffusion barrier between gold and silicon at temperatures as high as 360°C.

- Adhesion of Ti-W to gold or silicon oxides is degraded by barrier "stuffing". Good adhesion can be achieved by using as unstuffed Ti-W layer at the interfaces.

- Gold hillock formation caused by thermally induced strain can limit the life of gold metallizations. Passivation of the films with silicon nitride can retard this mechanism, as can deposition of the gold at elevated temperatures.

VIII. ACKNOWLEDGEMENTS

We are pleased to acknowledge the contributions to this project by D.P. Smith who was responsible for the metal depositions, O.N. Nalin who did much of the stress testing and SEM analysis, and T. Coutumas of Plasma-Therm who helped in the development of a passivation layer. This work was performed under Naval Research Laboratory contracts N00173-79-C-0010 and N0014-83-C-2393 and funded under the Naval Air Systems Command sponsorship.

IX. REFERENCES

1. J.E. Baker, R.J. Blattner, S. Nadel, C.A. Evans, and R.S. Nowicki, "Thermal Annealing Study of Au/Ti-W Metallization on Silicon," Thin Solid Films, Vol. 69, pp. 53-62, 1980.

2. D.J. LaCombe, D.C. Dening, and A. Christou, "A New Failure Mechanism in Thin Gold Films at Elevated Temperatures," in Proceedings of the 20th Annual International Reliability Physics Symposium, San Diego, California, pp. 81-87, 1982.

3. D. Pramanik, and A.N. Saxena, "VLSI Metallization Using Aluminum and its Alloys," Solid State Technology, pp. 127-138, January 1983.

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